## PROGRAMMABLE INPUT -OUTPUT PORT(8255)

- The parallel input-output port chip 8255 is also called as programmable *peripheral input-output port.* The Intel's 8255 is designed for use with Intel's 8-bit, 16-bit and higher capability microprocessors. It has 24 input/output lines which may individually programmed in two groups of twelve lines each, or three groups of eight lines. The two groups of I/O pins are named as Group A and Group B. Each of these two groups contains a subgroup of eight I/O lines called as 8-bit port and another subgroup of four lines or a 4-bit port. Thus Group A contains an 8-bit port A along with a 4-bit port. C upper.
- The port A lines are identified by symbols PA0-PA7 while the port C lines are identified as PC4-PC7. Similarly, Group B contains an 8-bit port B, containing lines PB0-PB7 and a 4-bit port C with lower bits PC0- PC3. The port C upper and port C lower can be used in combination as an 8-bit port C.
- The internal block diagram and the pin configuration of 8255 are shown in fig.
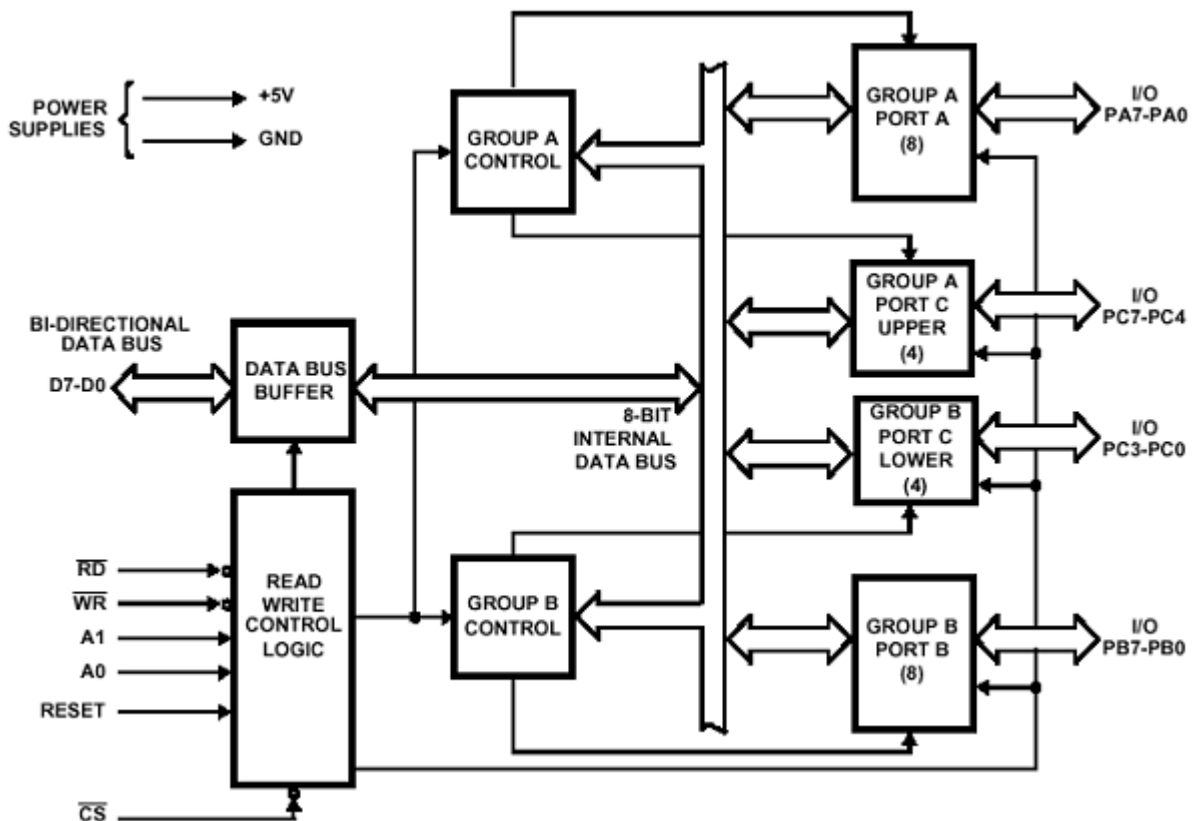
- The 8-bit data bus buffer is controlled by the read/write control logic. The read/write control logic manages all of the internal and external transfers of both data and control words
- RD, WR, A1, A0 and RESET are the inputs provided by the microprocessor to the READ/ WRITE control logic of 8255. The 8-bit, 3-state bidirectional buffer is used to interface the 8255 internal data bus with the external system data bus.
- This buffer receives or transmits data upon the execution of input or output instructions by the microprocessor. The control words or status information is also transferred through the buffer.

It has a 40 pins of 4 groups.

- 1. Data bus buffer
- 2. Read Write control logic
- 3. Group A and Group B controls
- 4. Port A, B and C

Data bus buffer: This is a tristate bidirectional buffer used to interface the 8255 to system databus. Data is transmitted or received by the buffer on execution of input or output instruction by the CPU. Control word and status information are also transferred through this unit.

Read/Write control logic: This unit accepts control signals (RD, WR) and also inputs from address bus and issues commands to individual group of control blocks (Group A, Group B).

$\overline{CS}$ – Chip select : A low on this PIN enables the communication between CPU and 8255

$\overline{RD}$ (Read) – A low on this pin enables the CPU to read the data in the ports or the status word through data bus buffer.

$\overline{WR}$ (Write) : A low on this pin, the CPU can write data on to the ports or on to the control register through the data bus buffer.

Group A and Group B controls : These block receive control from the CPU and issues commands to their respective ports

Group A - PA and PCU (PC7 –PC4)

Group B - PCL (PC3 – PC0)

Control word register can only be written into no read operation of the CW register is allowed

Port A: This has an 8 bit latched/buffered O/P and 8 bit input latch. It can be programmed in 3 modes – mode 0, mode 1, mode 2.

Port B: This has an 8 bit latched / buffered O/P and 8 bit input latch. It can be programmed in mode 0, mode1.

Port C : This has an 8 bit latched input buffer and 8 bit out put latched/buffer. This port can be divided into two 4 bit ports and can be used as control signals for port A and port B. it can be programmed in mode 0.

Signal Description

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       PA3 | 1        40 | PA4
       PA2 | 2        39 | PA5
       PA1 | 3        38 | PA6
       PA0 | 4        37 | PA7
        RD | 5        36 | WR
        CS | 6        35 | RESET
       gnd | 7        34 | D0
        A1 | 8        33 | D1
        A0 | 9        32 | D2
       PC7 | 10  8255 31 | D3
       PC6 | 11  PPI  30 | D4
       PC5 | 12       29 | D5
       PC4 | 13       28 | D6
       PC0 | 14       27 | D7
       PC1 | 15       26 | Vcc
       PC2 | 16       25 | PB7
       PC3 | 17       24 | PB6
       PB0 | 18       23 | PB5
       PB1 | 19       22 | PB4
       PB2 | 20       21 | PB3
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The signal description of 8255 are briefly presented as follows :

PA 7-PA 0: These are eight port A lines that acts as either latched output or buffered input lines depending upon the control word loaded into the control word register.

PC 7-PC 4 : Upper nibble of port C lines. They may act as either output latches or input buffers lines. This port also can be used for generation of handshake lines in mode 1 or mode 2.

PC 3-PC 0 : These are the lower port C lines, other details are the same as PC 7-PC 4 lines.

PB 0-PB 7 : These are the eight port B lines which are used as latched output lines or buffered input lines in the same way as port A.

$\overline{RD}$: This is the input line driven by the microprocessor and should be low to indicate read operation to 8255

$\overline{WR}$: This is an input line driven by the microprocessor. A low on this line indicates write operation.

$\overline{CS}$: This is a chip select line. If this line goes low, it enables the 8255 to respond to RD and WR signals, otherwise RD and WR signal are neglected

A 1-A 0 : These are the address input lines and are driven by the microprocessor. These lines A1-A 0 with RD, WR and CS from the following operations for 8255. These address lines are used for addressing any one of the four registers, i.e. three ports and a control word register as given in table below.

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	Input (Read) cycle
0	1	0	0	0	Port A to data bus
0	1	0	0	1	Port B to data bus
0	1	0	1	0	Port C to data bus
0	1	0	1	1	CWR to data bus

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	Output (Write) cycle
1	0	0	0	0	Data bus to Port A
1	0	0	0	1	Data bus to Port B
1	0	0	1	0	Data bus to Port C
1	0	0	1	1	Data bus to CWR

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	Function
X	X	1	X	X	Data bus tristated
1	1	0	X	X	Data bus tristated

**D0-D7** : These are the data bus lines those carry data or control word to/from the microprocessor.

 RESET : A logic high on this line clears the control word register of 8255. All ports are set as input ports by default after reset.

Modes of Operation of 8255

- These are two basic modes of operation of 8255. **I/O mode** and **Bit Set-Reset mode (BSR).**
- In **I/O mode**, the 8255 ports work as programmable I/O ports, while in BSR mode only port C (PC0-PC7) can be used to set or reset its individual port bits.
- Under the I/O mode of operation, further there are three modes of operation of 8255, so as to support different types of applications, mode 0, mode 1 and mode 2.

BSR Mode: In this mode any of the 8-bits of port C can be set or reset depending on D0 of the control word. The bit to be set or reset is selected by bit select flags B3, B2 and B1 of the CWR as given in table

| B_3	B_2	B_1	Selected Bits of port C
0	0	0	B_0
0	0	1	B_1
0	1	0	B_2
0	1	1	B_3
1	0	0	B_4
1	0	1	B_5
1	1	0	B_6
1	1	1	B_7

B_3, B_2, B_1, are from 000 to 111 for bits PC_0 to PC_7
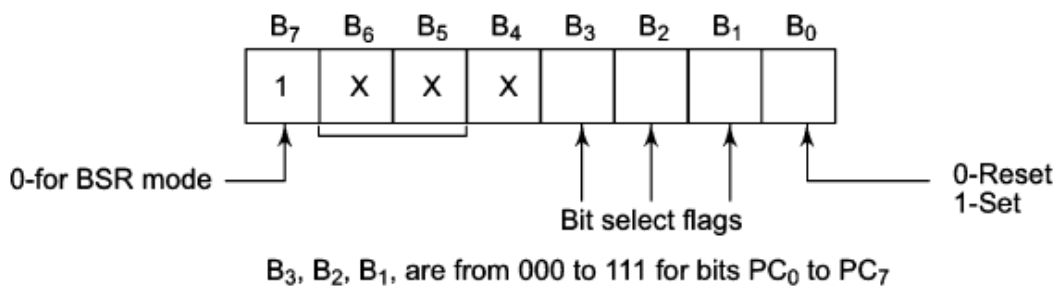
BSR Mode Control Word Register Format

I/O Modes

Mode 0 (Basic I/O mode): This mode is also called as basic input/output mode. This mode provides simple input and output capabilities using each of the three ports. Data can be simply read from and written to the input and output ports respectively, after appropriate initialisation

The salient features of this mode are as listed below:

1. Two 8-bit ports (port A and port B)and two 4-bit ports (port C upper and lower) are available. The two 4-bit ports can be combinedly used as a third 8-bit port.

2. Any port can be used as an input or output port.

3. Output ports are latched. Input ports are not latched.

4. A maximum of four ports are available so that overall 16 I/O configuration are possible.

• All these modes can be selected by programming a register internal to 8255 known as CWR.

I/O Mode Control Word Register Format
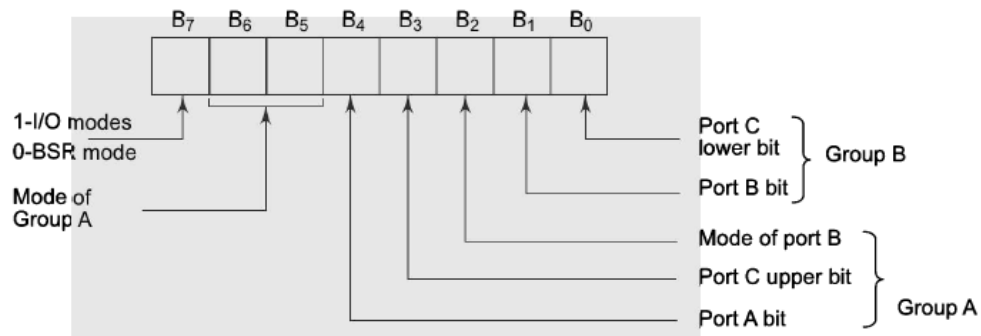
Group A modes

B_6	B_5	Mode
0	0	mode 0
0	1	mode 1
1	0	mode 2
1	1	x

(i) Port B mode is either 0 or 1 depending upon B2 bit.

(ii) A port is an output port if the port bit is 0 else it is input port

Mode 1: *(Strobed input/output mode):* In this mode the handshaking control the input and output action of the specified port. Port C lines PC0-PC2, provide strobe or handshake lines for port B. This group which includes port B and PC0-PC2 is called as group B for Strobed data input/output. Port C lines PC3-PC5 provide strobe lines for port A. This group including port A and PC3-PC5 from group A. Thus port C is utilized for generating handshake signals.

The salient features of mode 1 are listed as follows:

1. Two groups – group A and group B are available for strobed data transfer.

2. Each group contains one 8-bit data I/O port and one 4-bit control/data port.

3. The 8-bit data port can be either used as input and output port. The inputs and outputs both are latched.

4. Out of 8-bit port C, PC0-PC2 are used to generate control signals for port B and PC3-PC5 are used to generate control signals for port A. the lines PC6, PC7 may be used as independent data lines.

The control signals for both the groups in input and output modes are explained as follows:

Input control signal definitions (mode 1):

$\overline{STB}$(Strobe input) – If this lines falls to logic low level, the data available at 8-bit input port is loaded into input latches.

IBF (Input buffer full) – If this signal rises to logic 1, it indicates that data has been loaded into latches, i.e. it works as an acknowledgement. IBF is set by a low on STBand is reset by the rising edge of RD input.

INTR (Interrupt request) – This active high output signal can be used to interrupt the CPU whenever an input device requests the service. INTR is set by a high STB pin and a high at IBF pin. INTE is an internal flag that can be controlled by the bit set/reset mode of either PC4(INTEA) or PC2(INTEB) as shown in fig.
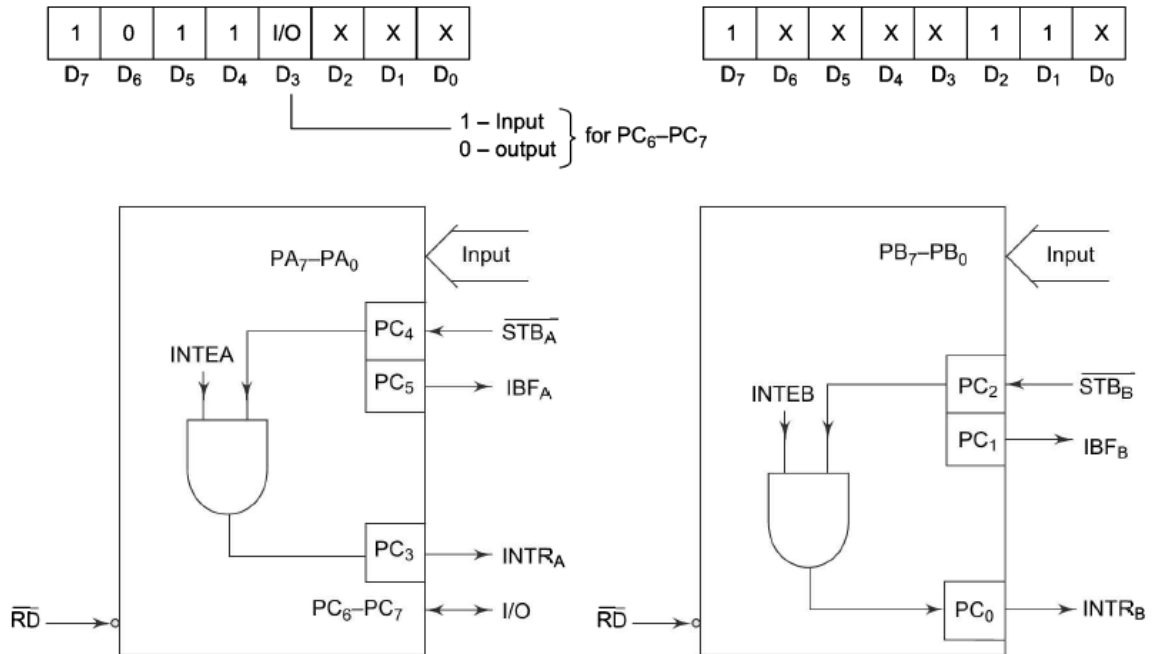
Fig. 5.27   (a) Mode1 Control Word Group A I/P (b) Mode 1 Control Word Group B I/P

INTR is reset by a falling edge of RD input. Thus an external input device can be request the service of the processor by putting the data on the bus and sending the strobe signal.
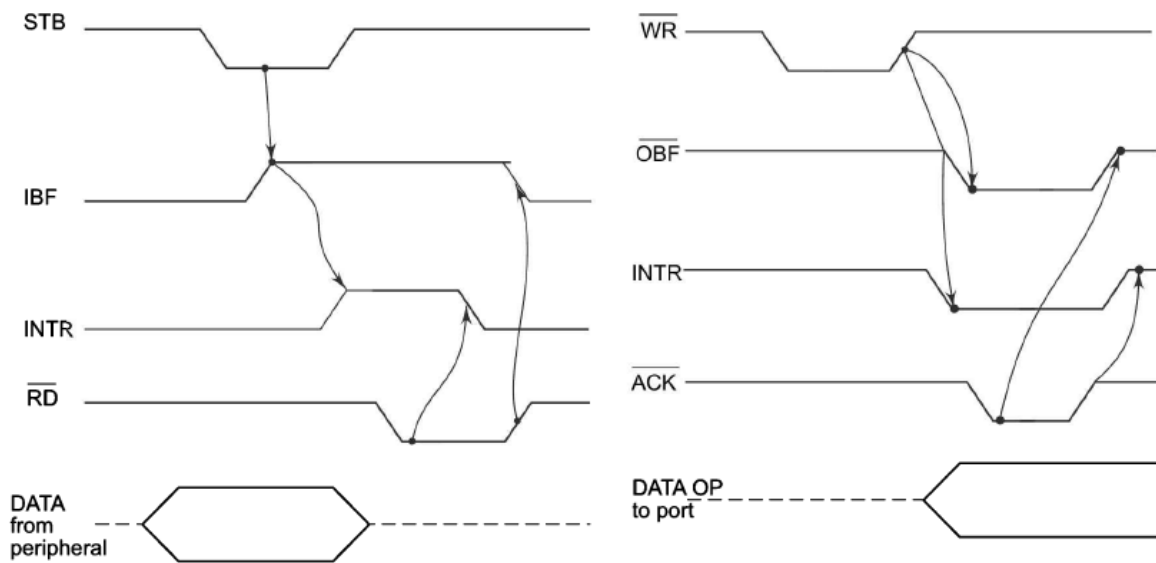
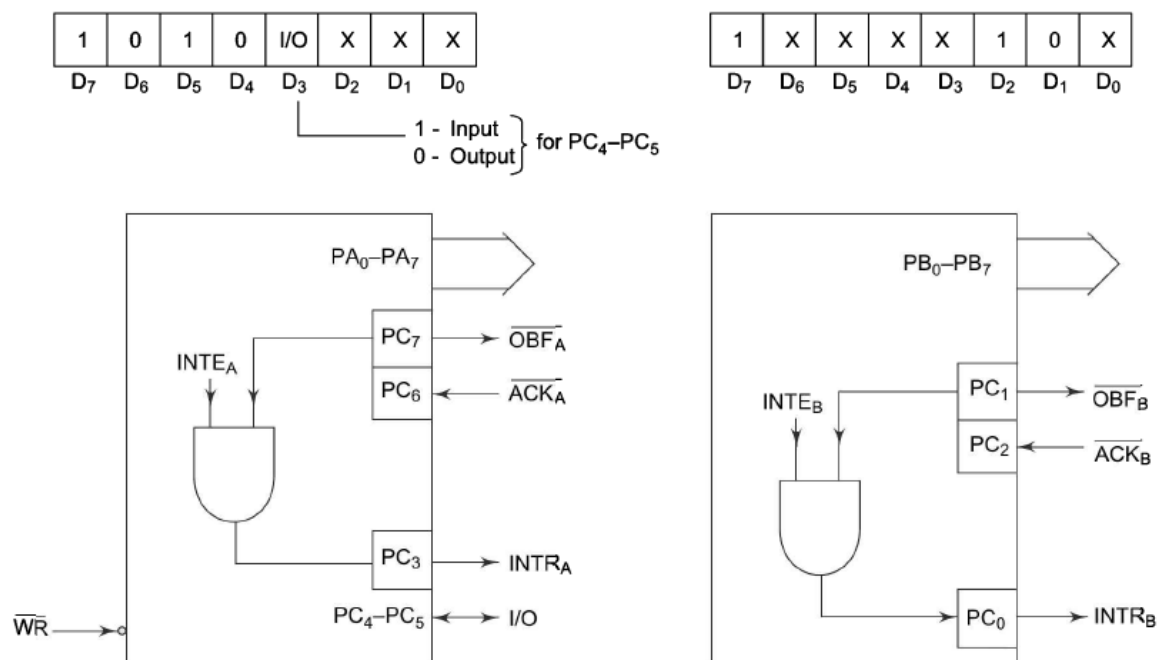(a) Mode1 Strobed Input Data Transfer (b) Mode1 Strobed Data Output

Fig. 5.29 (a) Mode 1 Control Word Group A o/p (b) Mode 1 Control Word Group B o/p

Output control signal definitions (mode 1) :

$\overline{OBF}$ (Output buffer full) – This status signal, whenever falls to low, indicates that CPU has written data to the specified output port. The OBF flip-flop will be set by a rising edge of WR signal and reset by a low going edge at the ACK input.

$\overline{ACK}$ (Acknowledge input) – ACK signal acts as an acknowledgement to be given by an output device. ACK signal, whenever low, informs the CPU that the data transferred by the CPU to the output device through the port is received by the output device.

INTR (Interrupt request) – Thus an output signal that can be used to interrupt the CPU when an output device acknowledges the data received from the CPU. INTR is set when ACK, OBF and INTE are 1. It is reset by a falling edge on WR input. The INTEA and INTEB flags are controlled by the bit set-reset mode of PC6 and PC2 respectively.

Mode 2 *(Strobed bidirectional I/O):*This mode of operation of 8255 is also called as strobed bidirectional I/O. This mode of operation provides 8255 with an additional features for communicating with a peripheral device on an 8-bit data bus. Handshaking signals are provided to maintain proper data flow and synchronization between the data transmitter and receiver. The interrupt generation and other functions are similar to mode 1.

- In this mode, 8255 is a bidirectional 8-bit port with handshake signals. The RD and WR signals decide whether the 8255 is going to operate as an input port or output port

The Salient features of Mode 2 of 8255 are listed as follows:

1. The single 8-bit port in group A is available.

2. The 8-bit port is bidirectional and additionally a 5-bit control port is available.

3. Three I/O lines are available at port C.(PC2 – PC0)

4. Inputs and outputs are both latched.

5. The 5-bit control port C (PC3-PC7) is used for generating / accepting handshake signals for the 8-bit data transfer on port A.

Control signal definitions in mode 2:

INTR – (Interrupt request) As in mode 1, this control signal is active high and is used to interrupt the microprocessor to ask for transfer of the next data byte to/from it. This signal is used for input (read) as well as output (write) operations.

Control Signals for Output operations:

$\overline{OBF}$ (Output buffer full) – This signal, when falls to low level, indicates that the CPU has written data to port A.

$\overline{ACK}$ (Acknowledge) This control input, when falls to logic low level, acknowledges that the previous data byte is received by the destination and next byte may be sent by the processor. This signal enables the internal tristate buffers to send the next data byte on port A.

INTE1 (A flag associated with OBF) This can be controlled by bit set/reset mode with PC6.

Control signals for input operations :

$\overline{STB}$ (Strobe input) A low on this line is used to strobe in the data into the input latches of 8255.

IBF (Input buffer full) When the data is loaded into input buffer, this signal rises to logic '1'. This can be used as an acknowledge that the data has been received by the receiver.

The waveforms in fig show the operation in Mode 2 for output as well as input port. WR must occur before ACK and STB must be activated before RD.

The following fig shows a schematic diagram containing an 8-bit bidirectional port, 5-bit control port and the relation of INTR with the control pins. Port B can either be set to Mode 0 or 1 with port A(Group A) is in Mode 2.

• Mode 2 is not available for port B. The following fig shows the control word.

(a) Mode 2 pins (b) Mode 2 control word
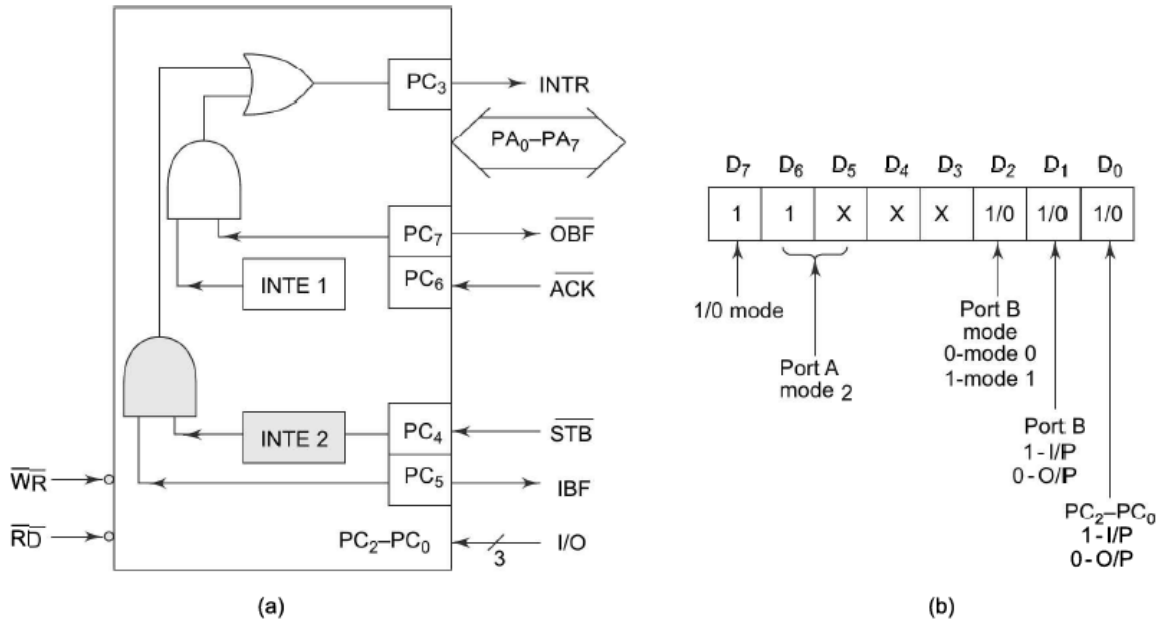
The INTR goes high only if either IBF, INTE2, STB and RD go high or OBF, INTE1, ACK and WR go high. The port C can be read to know the status of the peripheral device, in terms of the control signals, using the normal I/O instructions.
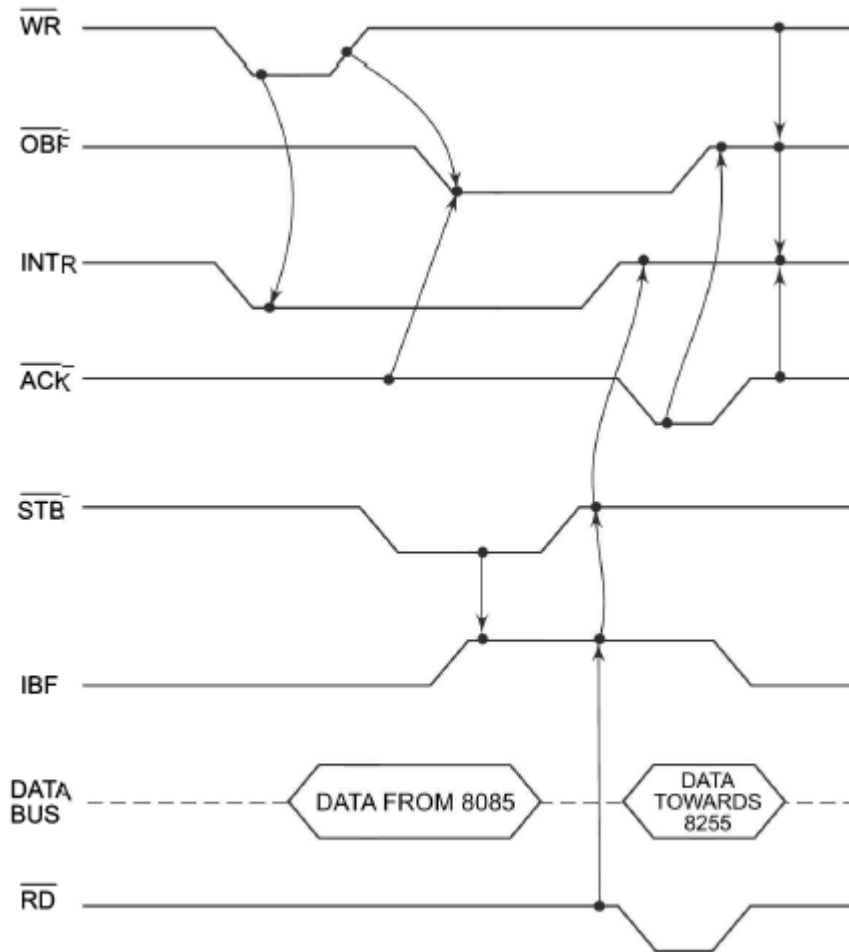
Mode 2 Bidirectional Data Transfer

REVIEW QUESTIONS

1. Explain the Mode 2 operation of 8255
2. Describe the control word format for the BSR mode of 8255.
3. With a neat diagram describe the architecture of 8255.
4. What are the three different I/O modes supported by 8255?
5. Mention the salient features of basic I/O mode operation of 8255.
6. Identify the mode and I/O configuration for ports A, B and C of an 8255 after its control register is loaded with 86 H?
7. Mention the salient features of basic I/O mode operation of 8255